ARGUMENTS/REMARKS

Favorable consideration of this application in view of the following remarks is respectfully requested.

Claims 1-18 are pending in the application.

In the outstanding Office Action, Claims 1 and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Oh et al. (U.S. Patent No. 6,200,903); Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Kobayashi (JP 4127518A); Claims 2 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Oh as applied to Claim 1 above, and further in view of Applicants' admitted prior art; Claims 2-4 were rejected under 35 U.S.C § 103(a) as being unpatentable over Oh or Kobayashi as applied to Claim 1 above, and further in view of Bell (U.S. Patent No. 5,767,018); Claims 9 and 10 were rejected under 35 U.S.C § 103(a) as being unpatentable over Oh as applied to Claim 1 above, and further in view of Geusic et al. (U.S. Patent No. 6,518,615); Claim 11 was rejected under 35 U.S.C § 103(a) as being unpatentable over Oh and Geusic as applied to Claim 9 above, and further in view of Borodovsky (U.S. Patent No. 4,529,685); and Claims 5, 6 and 12-18 were indicated as allowable.

Applicants gratefully acknowledge the indication of the allowable subject matter.

Applicants acknowledge with appreciation the interview between the Examiner and Applicants' representative on December 31, 2003. During the interview, the claims were reviewed in light of the disclosure surrounding Table 1 of the specification. Upon this review, the Examiner agreed that none of the cited references include any teaching or reference to critical dimension shift in a work pattern or any pre-determining of thickness relative to ion implantaion and critical dimension shift. The Examiner further agreed to consider withdrawing the pending rejections upon receipt of a formal response to the outstanding Official Action.

Briefly recapitulating, amended independent Claim 1 is directed to a method of manufacturing a semiconductor device, comprising steps of: (1) predetermining a first thickness of a first resist film and an ion implantation level that will cause the first thickness to contract to a second thickness. Once these values are determined, the method includes the steps of (a) forming an etching object on a semiconductor substrate; (b) forming the first resist film with the first predetermined thickness on the etching object; (c) patterning the first resist film to obtain a first resist pattern; (d) performing ion implantation into the first resist pattern with the predetermined ion implantation level set so that the first thickness contracts to the second thickness; and (e) etching on the etching object using the first resist pattern as a mask to obtain a work pattern, after execution of the steps (c) and (d). The second thickness of the first resist pattern includes a thickness satisfying such a condition that a difference in critical dimension shift in the work pattern with respect to the first resist pattern caused between a dense pattern portion and a rough pattern portion in the work pattern is not more than a predetermined reference value and causes no hindrance to the predetermined etching. Critical dimension shift is a phenomenon that varies with the density of the etching.[1] The critical dimension shift on a rough region having a relatively large space width differs from the critical dimension shift on a dense region having a relatively small space width.[2] By controlling the critical dimension shift in patterns with both high and low density portions, precise pattern etching of high density patterns is more easily achieved.[3]

By way of example, a thickness (corresponding to the claimed second thickness of the first resist pattern) of 334 nm results in a critical dimension shift density difference (the difference in critical dimension shift of the present invention) between the densest pattern (corresponding to the claimed dense pattern portion) and an isolated line pattern having a

[1] Specification, page 2, line 17 – page 3, line 15.
[2] Specification, page 2, lines 23-25.

sufficiently wide space (corresponding to the claimed rough pattern portion) of 0.059 μm (ΔCD2 in Fig. 12) which is less than 0.06 μm (corresponding to the claimed predetermined reference value). See Table 1 of the specification for further examples of Applicants' claimed critical dimension shift. Further, conventional shoulder drop (see Fig. 56) of the resist pattern does not take place during etching (corresponding to the claimed feature of offering no hindrance to the predetermined etching). Hence, Applicants' claimed thicknesses and ion implantation levels are not arbitrary but instead are predetermined to achieve a desired critical dimension shift and a beneficial purpose.

Oh is directed to a method of manufacturing a semiconductor device where a first photoresist pattern is hardened by argon implantation, where the tilt angle of argon implantation is controlled to prevent or minimize thickness contraction.[4] This process allows for thinner and harder first resist patterns, thus allowing second photoresist patterns to be applied more easily and without breakage of the first photoresist pattern.[5] As agreed by the Examiner during the interview of August 13, 2003, Oh does not, however, mention critical dimension shift let alone teach or suggest predetermining a first thickness of a first resist film and an ion implantation level that will cause the first thickness to contract to a second thickness as recited in amended Claim 1. Neither does Oh teach a second thickness of the first resist pattern includes a thickness satisfying such a condition that a difference in critical dimension shift in the work pattern with respect to the first resist pattern caused between a dense pattern portion and a rough pattern portion in the work pattern is not more than a predetermined reference value and causes no hindrance to the predetermined etching. Applicants submit that Oh only discloses background art where "by applying ion implantation, the thickness of the resist can be less by about 30-40% than for the

[3] Specification, page 6, lines 3-11.
[4] Oh, column 3, lines 24-44, Figure 6.

conventional case." By not predetermining ion implantation levels and thicknesses, the teachings of Oh do not teach Applicants' claimed inventions and do not result in a controlled critical dimension shift that prevents hindrances to etching.

Applicants therefore submit Oh does not teach or suggest all the features recited in amended Claim 1 and, thus, the inventions defined by independent Claim 1, and all claims depending therefrom, are not rendered obvious by the asserted prior art for at least the reasons stated above.[6]

Kobayashi teaches boron implantation to controllably contract a first resist film thickness.[7] However, like Oh, Kobayashi does not teach or suggest predetermining a first thickness of a first resist film and an ion implantation level that will cause the first thickness to contract to a second thickness. Neither does Kobayashi teach a second thickness of the first resist pattern includes a thickness satisfying such a condition that a difference in critical dimension shift in the work pattern with respect to the first resist pattern caused between a dense pattern portion and a rough pattern portion in the work pattern is not more than a predetermined reference value and causes no hindrance to the predetermined etching. Thus, Applicants submit that Kobayashi does not anticipate or render obvious the present invention for at least the reasons cited above.

Regarding the rejection of Claims 2 and 4, Applicants traverse the finding in the Official Action that "forming insulating film including silicon nitride is requisite in the conventional etching of the wiring pattern forming method as described in page 3, line 13, of the specification." Applicants disclosed conventional art only teaches silicon nitride as an

---

[5] Oh, column 4, lines 21-28.
[6] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."
[7] Kobayashi, page 6, line 15 – page 7, line 5.

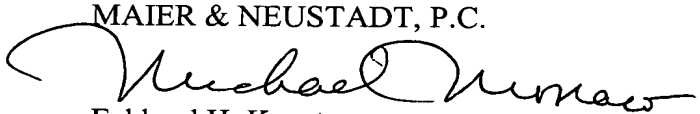
example of an insulating film to insulate metal wiring and so on. On the other hand, Applicants Claim 2 clearly recites that the ion prevention film prevents ions implanted in step (d) from being implanted into the actual etching object, and the ion prevention film is set for the purpose to prevent the ion implantation to the actual etching object. Therefore, the conventional use of a silicon nitride film for insulation does not rise to the level of a teaching or suggestion of forming a silicon nitride film on an actual etching object as an ion implantation prevention film. In addition, the anti-reflective coating disclosed by Applicants' disclosed prior art of Bell is a film mounted to prevent the desensitization by the reflection of the light, and is not mounted to prevent ion implantation as recited in Applicants' Claim 2. Hence, Applicants request the pending rejection of Claims 2 and 4 be withdrawn as both Applicants' disclosed prior art and Oh fail to teach or suggest the recited features of Claim 2.

Applicants have also considered the Bell, Geusic, and Borodovsky references and submit that these references do not cure the above-described deficiencies of Oh or Kobayashi.

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Michael E. Monaco
Registration No. 52,041

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
EHK/MEM/kkn
I:\ATTY\MM\AMENDMENT\0057\211909.AM.DUE MARCH 04.DOC